REMARKS

Status Of Application

Claims 1-15 are pending in the application; the status of the claims is as follows:

Claims 1-3 and 5-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,233,361 B1 to Downs ("Downs") and further in view of U.S. Patent No. 4,271,476 to Lotspiech ("Lotspiech").

Claim 4 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Amendments

Claim 1 has been amended to more explicitly require that the processors process different portions of the same image. Claim 5 has been amended to correct grammatical errors. These changes do not introduce any new matter.

35 U.S.C. § 103(a) Rejection

The rejection of claims 1-3 and 5-12 under 35 U.S.C. § 103(a), as being unpatentable over Downs and further in view of Lotspiech, is respectfully traversed because there can be no motivation to make the proposed combination, and because the combination fails to teach all elements of the subject claims.

Downs appears to teach a device designed to extract topographical information from a scene, such information subsequently being used for additional processing and computation, e.g., scene navigation. See Col. 21, lines 13 to 20. The device processes multiple views of a scene taken from six image sensors organized as three virtual cameras, plus a seventh image sensor that views the entire scene. See Figs. 3 and 5 and column 17,

line 40 'image sensor IS7" and line 47 "individual image sensors 1,2,3,4,5,6." The images are compared on a scanline basis to identify vectors to parts of the scene having common attributes. The result is a representation of the three dimensional topographic details of the scene. Column 21, lines 19-20. Thus, Downs is focused on processing images to extract three dimensional (3D) information.

Lotspiech teaches a method of processing one (1) digital image to rotate the scan format thereof. Specifically, Lotspiech teaches to subdivide a single image into sections; to decompress, rotate, and recompress the individual sections; and then reassemble the sections to form the rotated image. Thus, Lotspiech is directed to a manipulation of a two-dimensional (2D) image.

Of particular interest, Downs appears to process the composite video images on a scanline-by-scanline basis in real time. In contrast, Lotspiech operates on a compressed image stored in a memory. It is, therefore, unclear as to how the two references could be combined without altering the principles of operation of one or the other device. That is, Downs would have to be modified to operate on an image-by-image basis. However, where the modification changes the principles of operation of a device, then there can be no motivation to make the modification. MPEP 2143.02. Accordingly, there can be no motivation to combine Downs and Lotspiech as proposed in the Office Action, and the combination is improper.

Even assuming arguendo that the combination were proper, the combination of Downs and Lotspiech still fails to teach all elements of the claims. For example, claim 1 requires "a plurality of processors processing respective portions of the same input image data." That is, multiple processors that operate on a single image. In contrast, Downs appears to teach multiple processors each processing a corresponding image, e.g., IPT1/2/3 in Fig. 4, or a pair of images, e.g., CSY of Fig. 4.

Claim 1 also requires "an address memory storing address information related to a position of each portion of said input image data within said input image data..." It is

alleged at page 2 of the Office Action, that this element of claim 1 is taught by Downs at column 15, lines 57-65. It is respectfully submitted, however, that the cited passage refers to "line scan processors ... each performing ... multiple address identity transforms in the identity Transform Processors which compute the existence of specific vector pair intersections which are stored in dedicated parallel triple buffered ordered pair vector intercept buffers." That is, the passage appears to state that the "specific vector pair intersections" are stored in the buffers. No mention is made of an address memory or of storing address information for portions of an image as required by claim 1. It is further submitted that Lotspiech fails to teach this element of claim 1. Accordingly, claim 1 distinguishes the proposed combination.

Claims 2-5, 14 and 15 depend from claim 1. It is respectfully submitted, therefore, that claims 2-5 and 14-15 distinguish over the proposed combination of Downs and Lotspiech for at least the same reasons as provided above regarding claim 1.

Claim 6 recites a memory for storing "arrangement information." As provided above in respect of claim 1, neither Downs nor Lotspiech teaches such a memory, i.e., an address memory. Accordingly, it is respectfully submitted that claim 6 distinguishes over the proposed combination of Downs and Lotspiech.

Claims 7-10 depend from claim 6. It is respectfully submitted, therefore, that claims 7-10 distinguish over the proposed combination of Downs and Lotspiech for at least the same reasons as provided above regarding claim 6.

Claim 11 recites "storing information indicating arrangement of said divided image data relative to said input image." As provided above in regards to claim 1, neither Downs nor Lotspiech teach this element of claim 11. Accordingly, it is respectfully submitted that claim 11 distinguishes over the proposed combination of Downs and Lotspiech.

Claim 12 recites plural processors each having an "input image data port and input image address port" and "output image data port and an output image address port." It is

respectfully submitted that this element of claim 12 is not taught by either Downs nor Lotspiech. Accordingly, it is respectfully submitted that claim 12 distinguishes over the proposed combination of Downs and Lotspiech.

Accordingly, it is respectfully requested that the rejection of claims 1-3 and 5-12 under 35 U.S.C. § 103(a) as being unpatentable over Downs and further in view of Lotspiech, be reconsidered and withdrawn.

CONCLUSION

Wherefore, in view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

This Amendment does not increase the number of independent claims, does not increase the total number of claims, and does not present any multiple dependency claims. Accordingly, no fee based on the number or type of claims is currently due. However, if a fee, other than the issue fee, is due, please charge this fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document pursuant to 37 C.F.R. §§ 1.16 and 1.17, other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

By: _____

Michael J. DeHaemer
Registration No. 39,164
Attorney for Applicants

MJD/llb:jkk
SIDLEY AUSTIN BROWN & WOOD LLP
717 N. Harwood, Suite 3400
Dallas, Texas 75201
Direct: (214) 981-3335
Main: (214) 981-3300
Facsimile: (214) 981-3400
September 20, 2005

DA1 325442v.5